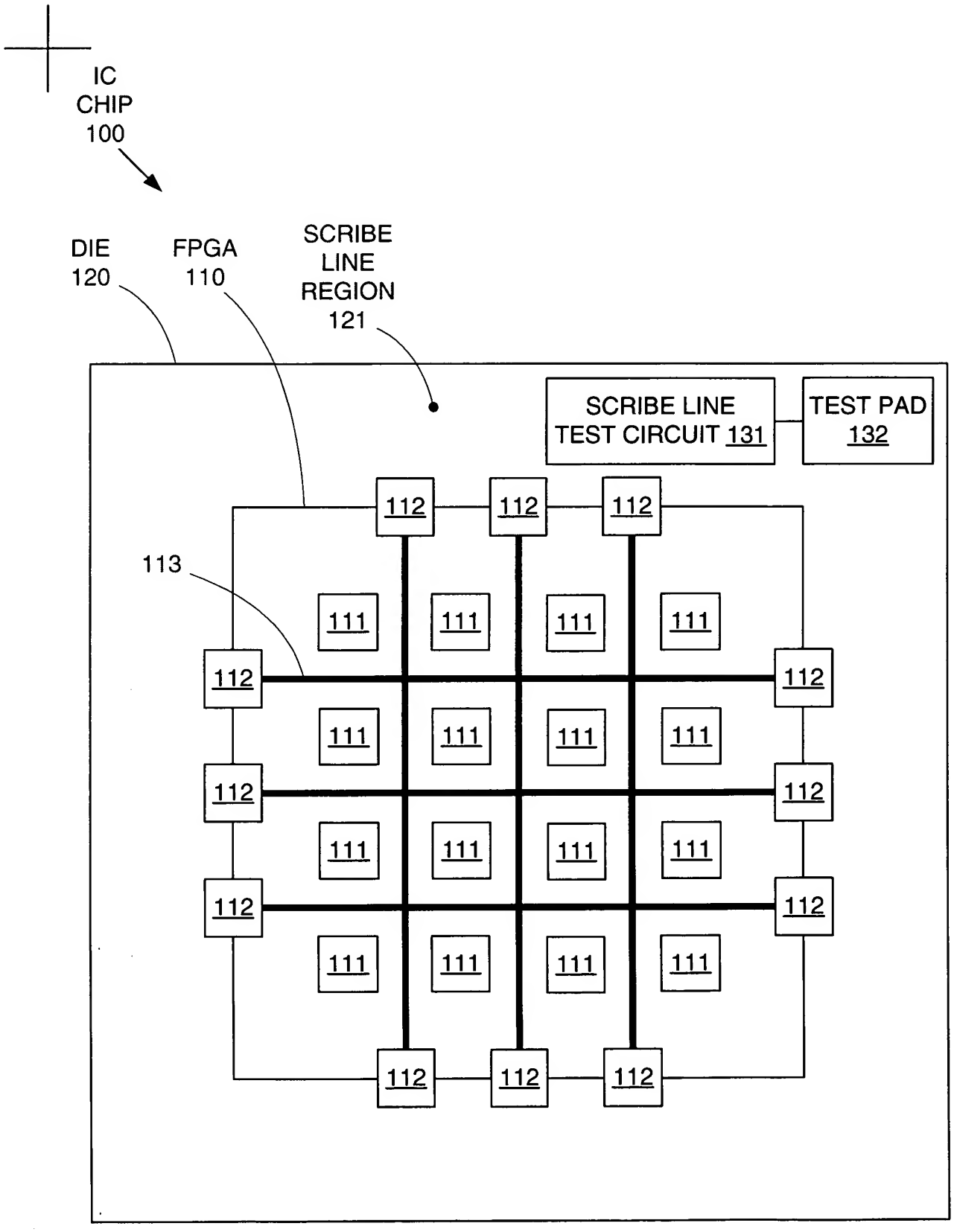


FIG. 1
(PRIOR ART)

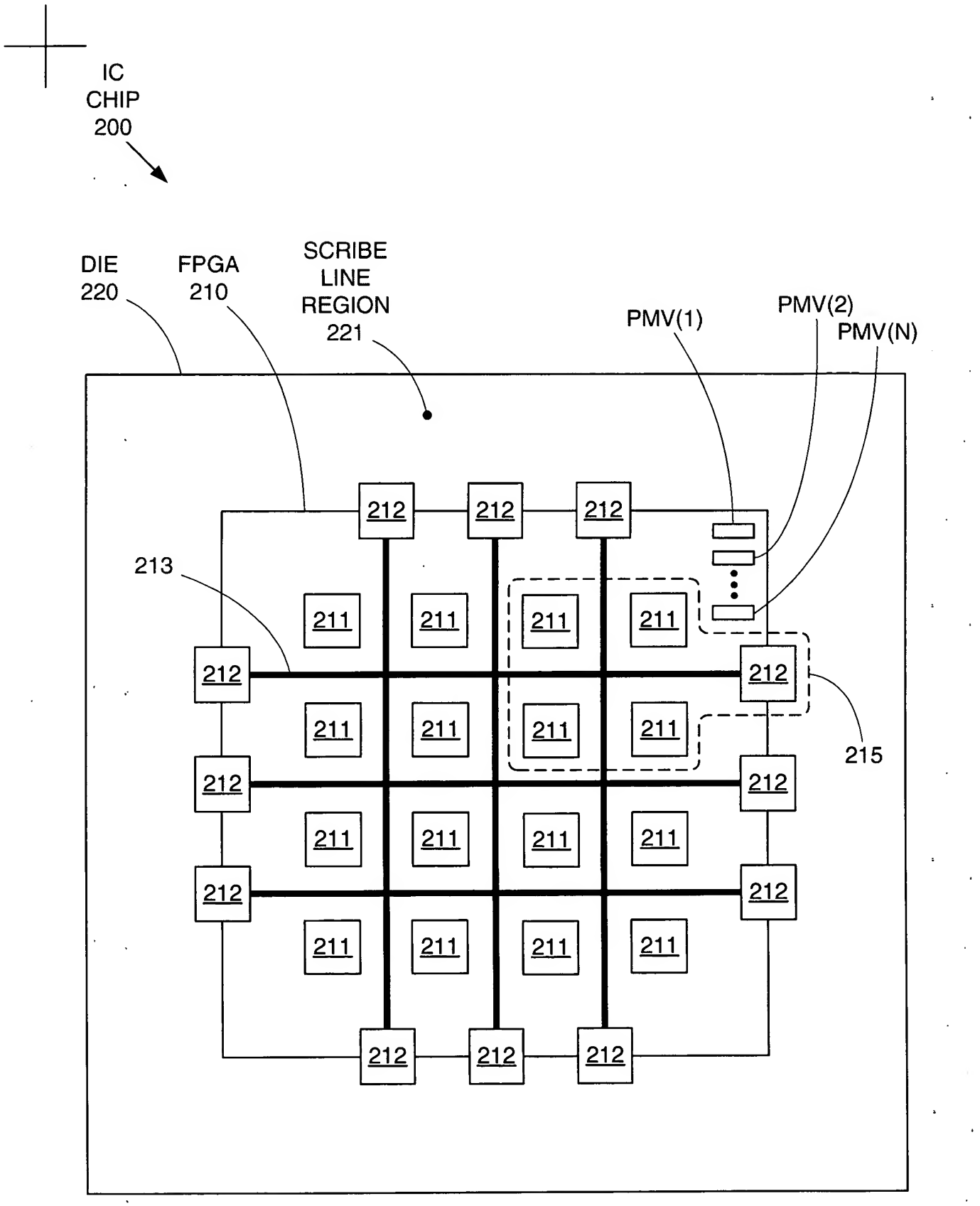

IC
CHIP
200
DIE
220
FPGA
210
SCRIBE
LINE
REGION
221
PMV(1)
PMV(2)
PMV(N)
213
212
211
215

FIG. 2

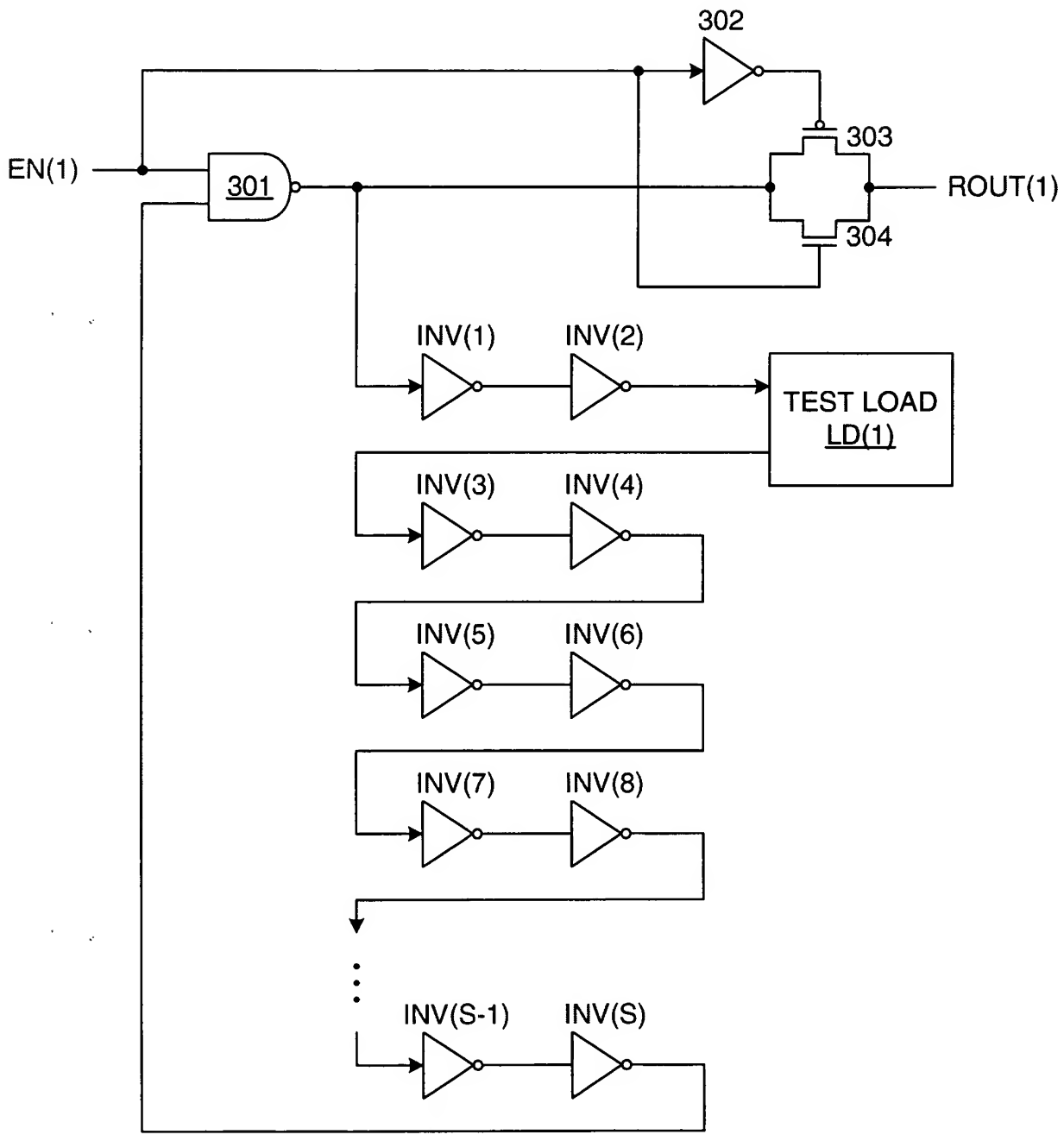

EMBEDDED
TEST CIRCUIT
PMV(1)
302
303
EN(1)
301
ROUT(1)
304
INV(1)
INV(2)
TEST LOAD
LD(1)
INV(3)
INV(4)
INV(5)
INV(6)
INV(7)
INV(8)
INV(S-1)
INV(S)

FIG. 3

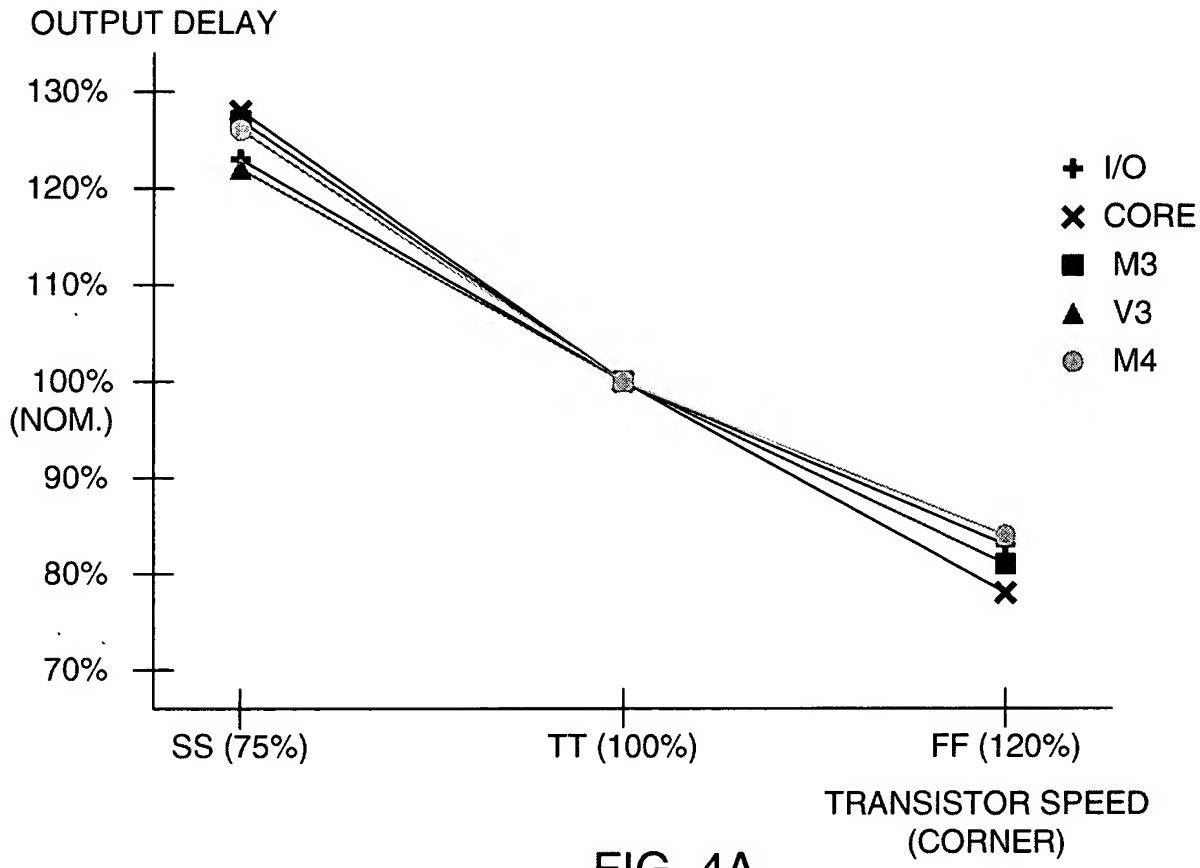

OUTPUT DELAY
130%
120%
110%
100%
(NOM.)
90%
80%
70%
SS (75%)
TT (100%)
FF (120%)
TRANSISTOR SPEED
(CORNER)
I/O
CORE
M3
V3
M4

FIG. 4A

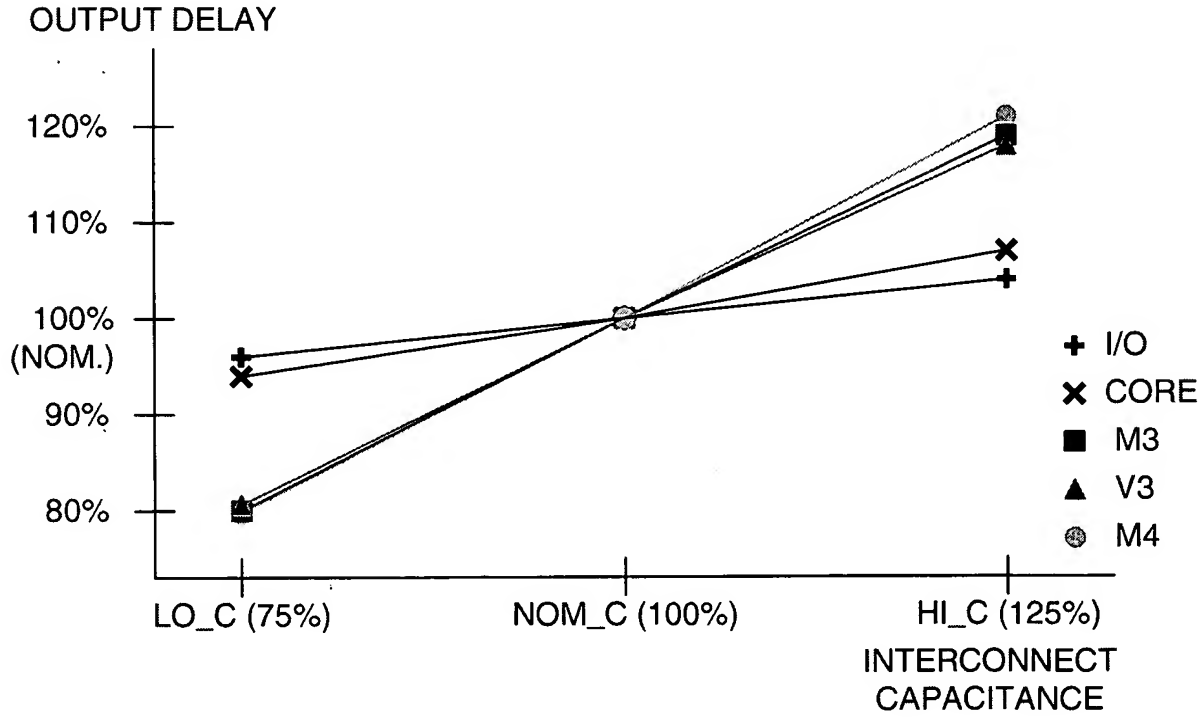
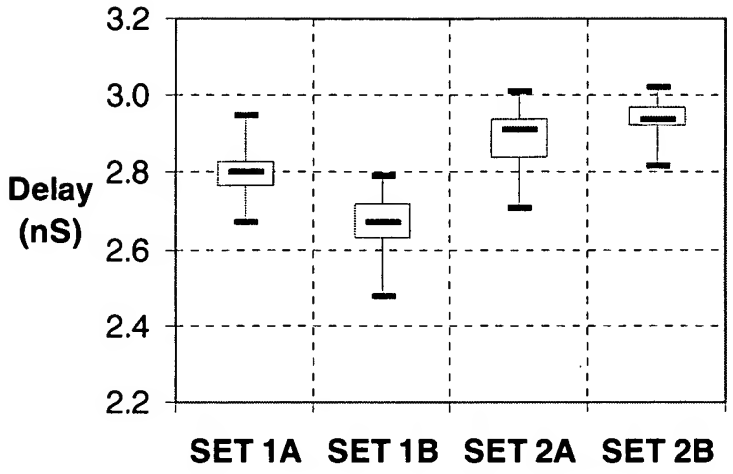
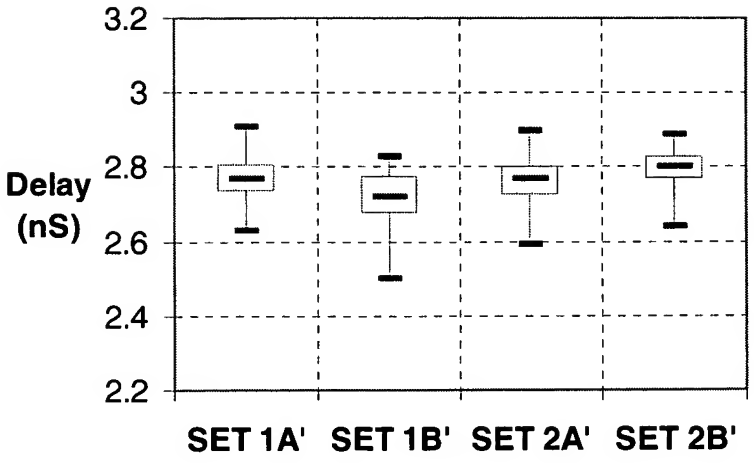

OUTPUT DELAY
120%
110%
100%
(NOM.)
90%
80%
LO_C (75%)
NOM_C (100%)
HI_C (125%)
INTERCONNECT
CAPACITANCE
I/O
CORE
M3
V3
M4

FIG. 4B



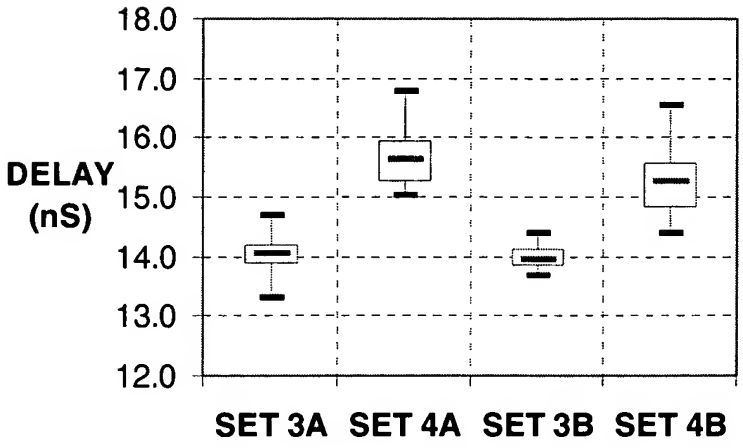
RAW FEOL DATA

FIG. 5A



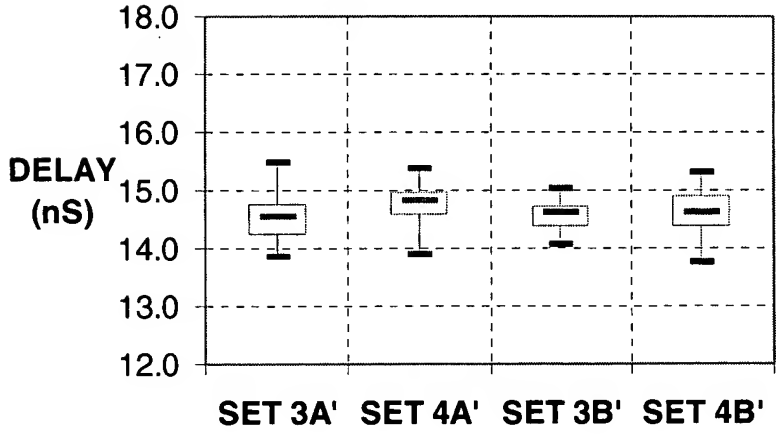
FEOL DATA AFTER BEOL EXTRACTION

FIG. 5B



RAW BEOL DATA

FIG. 6A



BEOL DATA AFTER FEOL EXTRACTION

FIG. 6B

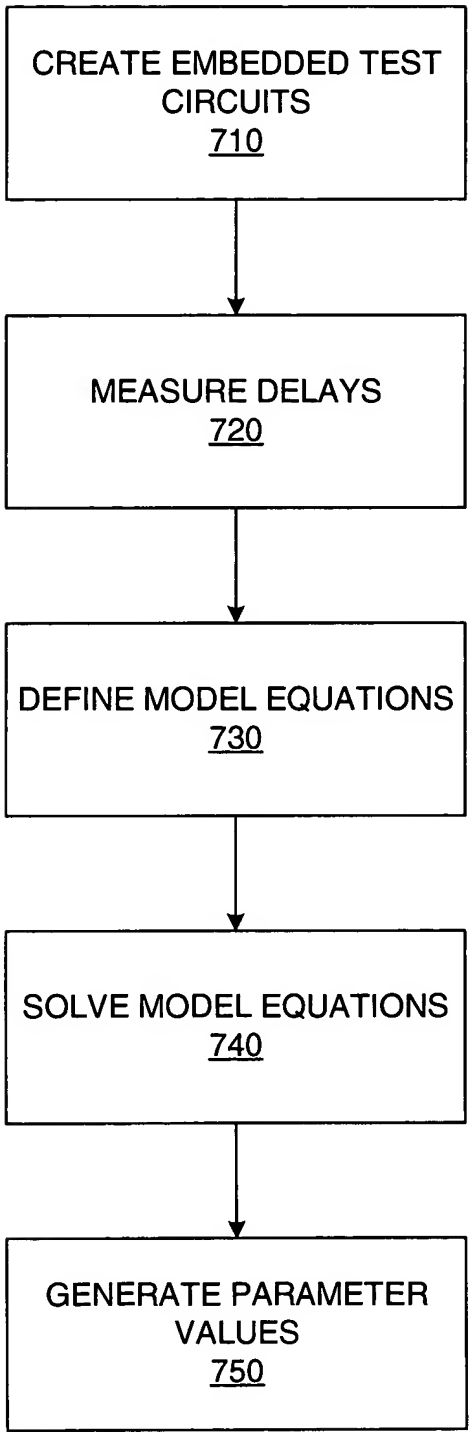

CREATE EMBEDDED TEST CIRCUITS
710
MEASURE DELAYS
720
DEFINE MODEL EQUATIONS
730
SOLVE MODEL EQUATIONS
740
GENERATE PARAMETER VALUES
750

FIG. 7